

U.S. Department of Energy
Office of Energy Efficiency and Renewable Energy
Advanced Materials and Manufacturing Technologies Office

NATIONAL LABORATORY CALL FOR PROPOSALS
Microelectronic Devices for Energy Efficiency Scaling

National Lab Funding for Fiscal Year 2023

DE-LC-0000023.0002

This Lab Call for proposals on Microelectronic Devices for Energy Efficiency Scaling is being issued by the U.S. Department of Energy's (DOE) Office of Energy Efficiency and Renewable Energy (EERE) Advanced Materials and Manufacturing Technologies Office (AMMTO).

Modifications

Mod. No.	Date	Description of Modification
0001	4/28/2023	Correct the email address for specific questions about this Lab Call throughout the lab call document. The correct email address is: micro.electronics@ee.doe.gov
0002	5/20/2023	Update the Full Application Submission Deadline to June 6, 2023

*Questions about this Lab Call? Email Micro.electronics@ee.doe.gov.
Problems with EERE eXCHANGE? Email ERE-eXCHANGESupport@hq.doe.gov.
Include Lab Call name and number in subject line.*

Table of Contents

I. Lab Call Description.....	3
A. Background and Context	3
i. Overview and Purpose	3
ii. Timeline and Process Logistics	6
Timeline.....	6
Process Logistics.....	6
B. Key Considerations and Topic Area	7
i. Key Considerations.....	7
ii. Topic Area Descriptions.....	9
Topic 1: Lab Seedlings for Devices that contribute at least 10X to EES2.....	9
II. Application Submission and Review Information.....	13
A. Application and Submission Details.....	13
i. Application Process	13
ii. General Proposal Requirements	14
iii. Proposal Content.....	14
Full Applications	14
Technical Volume.....	15
Resumes.....	19
Letters of Commitment (if applicable).....	19
Summary/Abstract for Public Release	19
Summary Slide	20
Budget for DOE/NNSA FFRDC (if applicable)	20
Authorization for non-DOE/NNSA or DOE/NNSA FFRDCs (if applicable).....	20
SF-LLL: Disclosure of Lobbying Activities.....	20
Waiver Requests: Foreign Entities and Foreign Work (if applicable)	21
Data Management Plan	21
Diversity, Equity, Inclusion, and Accessibility (DEIA) Implementation Plan	22
Treatment of Application Information.....	23
B. Application Review Details.....	24
i. Merit Review and Selection Process	24

Questions about this Lab Call? Email Micro_electronics@ee.doe.gov.

Problems with EERE eXCHANGE? Email EERE-eXCHANGESupport@hq.doe.gov.

Include Lab Call name and number in subject line.

ii. Technical Review Criteria	24
Final Applications	24
iii. Selection for Award Negotiation	26
iv. Selection Notification	26
v. Questions and Agency Contacts.....	26
Appendix A: Lab Call Full Application Worksheet for eXCHANGE	27
Appendix B: Waiver Requests and Approval Processes:.....	34
Appendix C: EERE Definition of Technology Readiness Levels.....	37

Questions about this Lab Call? Email Micro.electronics@ee.doe.gov.
Problems with EERE eXCHANGE? Email EERE-eXCHANGESupport@hq.doe.gov.
Include Lab Call name and number in subject line.

I. Lab Call Description

A. Background and Context

i. Overview and Purpose

Building a clean and equitable energy economy and addressing the climate crisis are top priorities of the Biden Administration. This Lab Call will advance the Administration’s goals to achieve carbon pollution-free electricity by 2035 and to “deliver an equitable, clean energy future, and put the United States on a path to achieve net-zero emissions, economy-wide, by no later than 2050”¹ to the benefit of all Americans. The Department of Energy (DOE) is committed to pushing the frontiers of science and engineering, catalyzing clean energy jobs through research, development, demonstration, and deployment (RDD&D), and ensuring environmental justice and inclusion of underserved communities.²

In this Lab Call the terms “microelectronics” and/or “semiconductor” are used to refer to semiconductors and related materials, processing chemistries, design, fabrication, lithography, packaging, sensors, devices, integrated circuits, processors, computing architectures, modeling and simulation, software tools, and related technologies.

The research and development (R&D) activities to be funded under this Lab Call will support the government-wide approach to the climate crisis by driving the innovation that can lead to the deployment of clean energy technologies, which are critical for climate protection. Specifically, this Lab Call will be a critical element of an effort within DOE’s Office of Energy Efficiency and Renewable Energy (EERE) with goals to simultaneously spur technology leadership in microelectronics -- a foundational technology for clean energy -- and to stop exponential growth in microelectronics energy use. Achieving the former goal will accelerate and lower costs of innovation needed to achieve carbon pollution-free electricity by 2035; achieving the latter goal will prevent a spike in GHG emissions in the near term and also avoid strain on the

¹ Executive Order 14008, “Tackling the Climate Crisis at Home and Abroad,” January 27, 2021.

² The term “underserved communities” refers to populations sharing a particular characteristic, as well as geographic communities, that have been systematically denied a full opportunity to participate in aspects of economic, social, and civic life, as exemplified by the list in the definition of “equity.” E.O. 13985. For purposes of this Lab Call, as applicable to geographic communities, applicants can refer to economically distressed communities identified by the Internal Revenue Service as Qualified Opportunity Zones; communities identified as disadvantaged or underserved communities by their respective States; communities identified on the Index of Deep Disadvantage referenced at <https://news.umich.edu/new-index-ranks-americas-100-most-disadvantaged-communities/>, and communities that otherwise meet the definition of “underserved communities” stated above.

electricity grid as the economy evolves rapidly towards microelectronics-dependent net zero technologies in all sectors by 2050.

President Biden has recognized the economic and national security importance of microelectronics by signing into law and implementing the CHIPS and Science Act of 2022³. This Act appropriates more than \$60B for the semiconductor industry including more than \$11B for microelectronics related R&D at Department of Commerce's National Institute of Standards and Technology (NIST), Department of Defense (DOD) and the National Science Foundation (NSF). It is precisely because of this new substantial government-wide investment and new leadership in microelectronics R&D strategy that DOE is able to utilize investment in energy efficient microelectronic devices to have a major impact on the energy efficiency of microelectronics.

For decades, DOE has been at the leading edge of microelectronics as a consumer, as an engine of scientific understanding, and as a catalyst for deployment; all of which have enabled technological breakthroughs adopted by industry. Within DOE EERE's portfolio, both energy efficiency technologies, such as LED lighting and variable speed motors, and renewable energy technologies, ranging from the smallest solar cell to the largest wind turbine, are enabled by microelectronics.

Today, however, microelectronics themselves must become more energy efficient. The combination of the end of automatic energy efficiency increases due to Moore's Law⁴ and the exponential increase in energy use by new computing, sensing and other microelectronics workloads have made microelectronics a major and rapidly growing category of energy use. From 2010 to 2020, this combination of factors caused microelectronic energy use to double every three years, and since 2020, microelectronics energy use has increased beyond 10% of global electricity use. This unsustainable trend has created an unprecedented need for rapid increases in microelectronics energy efficiency for everything from nanoscale devices to artificial intelligence software. As a result, over the past three years, EERE's Advanced Materials and Manufacturing Technologies Office (AMMTO) has begun to build an agenda on R&D for ultra-energy efficient microelectronic devices.

³ [FACT SHEET: CHIPS and Science Act Will Lower Costs, Create Jobs, Strengthen Supply Chains, and Counter China](#)

⁴ Moore's Law refers to the trend observed by founding Intel CEO Gordon Moore in the 1970s that the number of transistors on a chip doubles every two years. While not a law of physics, Moore's observation held true for more than 45 years from the very first integrated circuits (IC) chips in the 1970s to the present day and therefore became known as a Moore's law. It is credited by microelectronics industry observers as being a fundamental driver for R&D advances and R&D planning during this time. Until 2010, the miniaturization resulting from Moore's law reduced the energy use by transistor proportionately, and energy use per bit in transistors halved every 2 years from the 1970s until 2010 when quantum effects that started becoming more important below 60 nanometers slowed energy benefits and changed miniaturization from a 2-dimensional to a 3-dimensional effort.

This Lab Call is focused on flattening the slope of microelectronics energy use as part of AMMTO's broader microelectronics R&D Roadmapping effort now called "Energy Efficiency Scaling for two Decades" (EES2).

While NIST and DOD stakeholders have long advocated on the economic and national security importance of microelectronics R&D, it is only in recent years that the urgent need for R&D on microelectronics energy efficiency has become apparent. AMMTO has taken the lead on creating the voluntary industry government microelectronics partnership called for in DOE's Semiconductor Supply Chain Report⁵ and has announced a [pledge](#) that has now been signed by forty-four other organizations to cooperate on RD&D for a new type of microelectronics' EES2. Similar to previous "Moore's law" scaling, this EES2 leads to the doubling of microelectronics' energy efficiency every two years. The two decades of EES efficiency doubling will be a 10 generation/20-year effort that leads to 1000X efficiency improvement that will prevent harmful impacts of microelectronics energy use. As part of the pledge, the signers agreed to cooperate with AMMTO on version 1.0 of an industry-government EES2 RD&D Roadmap slated to be complete by December 2023, and thereafter updated biennially.

The EES2 RD&D Roadmapping itself was launched on November 16, 2022 with the formation of seven working groups including the Materials and Devices Working Group.⁶ A [prior AMMTO workshop](#) informed the deliberations of this device-oriented group and it rapidly converged on a set of technologies of interest for at least 10x efficiency doubling that are shown in Table 1 of Topic 1 below. These devices are the focus of this Lab Call because they have already been proven at the lab scale and are foundational to microelectronics energy efficiency. The intent of this Lab Call is to support manufacturing and other R&D on prototype devices to advance them to at least technology readiness level⁷ (TRL) 6 where they are ready to be matured and commercialized in lab/industry partnerships.

In addition, this Lab Call will emphasize increasing diversity of research staff, increasing diversity of voices in research design, and or increasing quantification and emphasis on supporting underserved communities.

⁵ This report, known as DOE's "Semiconductor Supply Chain Deep Dive Assessment" was a component of the White House announcement on its 1-year Supply Chain Reports <https://www.energy.gov/sites/default/files/2022-02/Semiconductor%20Supply%20Chain%20Report%20-%20Final.pdf>.

⁶ The other six EES2 RD&D Roadmap working groups are: b-Circuits and Architectures, c-Heterogeneous Integration and Advanced Packaging, d-Algorithms and Software, e-Metrology and Benchmarking, f-Power and Control Electronics, and g-Manufacturing Energy Efficiency and Sustainability.

⁷ See Appendix C for EERE's definitions of the various TRL levels.

ii. Timeline and Process Logistics

Timeline

KEY DATES	
Lab Call Release Date:	April 19, 2023
PROPOSAL DEADLINE AND DECISION DATES	
Full Application Submission Deadline(s):	June 6, 2023 5:00 PM ET
Expected Decision Date(s):	July TBD
Expected Beginning Award Issue Date(s):	August TBD

Process Logistics

All communication to AMMTO regarding this Lab Call must use
Micro.electronics@ee.doe.gov.

- **PROPOSAL SUBMISSIONS:** To apply to this Lab Call, lab personnel must register (and sign in) with their lab email address and submit application materials through EERE eXCHANGE. Application materials must be submitted through EERE eXCHANGE at <https://eere-eXCHANGE.energy.gov>, EERE's online application portal. Frequently asked questions for this Lab Call and the EERE Application process can be found at <https://eere-eXCHANGE.energy.gov/FAQ.aspx>.

Applicants are responsible for meeting the submission deadlines. DOE strongly encourages all applicants to submit the required information at least 24 hours in advance of the submission deadline. Applicants should not wait until the last minute—internet and data server traffic can be heavy in the last hours before the submission deadline, which may affect the applicants' ability to successfully submit the required information before the deadline.

- **QUESTIONS DURING OPEN LAB CALL PERIOD:** Specific questions about this Lab Call should be submitted via e-mail to Micro.electronics@ee.doe.gov. AMMTO will provide answers related to this Lab Call on EERE eXCHANGE at: <https://eere-eXCHANGE.energy.gov>. Please note that you must first select the specific opportunity number for this Lab Call in order to view the questions and answers specific to this Lab Call. EERE will attempt to respond to a question within 3 business days, unless a similar question and answer have already been posted on the website.

Questions related to the registration process and use of the EERE Exchange website should be submitted to: EERE-eXCHANGESupport@hq.doe.gov. To ensure fairness for all lab participants, please do not ask individual AMMTO staff questions directly.

Questions about this Lab Call? Email Micro.electronics@ee.doe.gov.

Problems with EERE eXCHANGE? Email EERE-eXCHANGESupport@hq.doe.gov.

Include Lab Call name and number in subject line.

- **NOTIFICATION OF SELECTION:** When selections are finalized, lab leads will receive an email from Micro.electronics@ee.doe.gov.

B. Key Considerations and Topic Area

i. Key Considerations

- **AVAILABLE FUNDING:** There is approximately **\$4 million** in annual funding available to fund **all** projects solicited in this Lab Call pending appropriations, program direction, and go/no-go decision points.
- **NON-LAB PARTNERS:** A FFRDC or a National Laboratory may propose partnering with industry, academia or other non-lab entities to perform work under this Lab Call. Unless a waiver (see Appendix B) is approved by DOE, any partner must be organized and chartered or incorporated (or otherwise formed) under the laws of a state or territory of the United States; have majority domestic ownership and control; and have a physical location for business operations in the United States. The FFRDC or National Laboratory must enter into a CRADA or other written agreement approved by DOE with the partners prior to performing work under this Lab Call.
- **EXISTING PROJECTS:** Labs with existing projects addressing any of the topic areas below may incorporate that work in proposals they submit in response to this Lab Call to demonstrate existing capability and leverage existing partnerships with industry and other partners. If the proposal is not selected for funding under this Lab Call, the work under the existing projects will not be negatively impacted.
- **ELIGIBILITY:** DOE/National Nuclear Security Agency (NNSA) Federally Funded Research and Development Centers (FFRDCs), and all DOE/NNSA National Laboratories that have signed AMMTO's [Microelectronics Energy Efficiency Scaling for 2 Decades \(EES2\) Cooperation Pledge](#) are eligible to submit proposals. Proposals that involve more than one laboratory are also allowed. Only one proposal per Lab can be submitted to this Lab Call. Given available funding limits, multilab proposals are not encouraged.
- **DIVERSITY, EQUITY, INCLUSION and ACCESSIBILITY (DEIA):**
It is the policy of the Biden Administration that:
[T]he Federal Government should pursue a comprehensive approach to advancing equity⁸ for all, including people of color and others who have

⁸ The term “equity” means the consistent and systematic fair, just, and impartial treatment of all individuals, including individuals who belong to underserved communities that have been denied such treatment, such as Black, Latino, and Indigenous and Native American persons, Asian Americans and Pacific Islanders and other

been historically underserved, marginalized, and adversely affected by persistent poverty and inequality. Affirmatively advancing equity, civil rights, racial justice, and equal opportunity is the responsibility of the whole of our Government. Because advancing equity requires a systematic approach to embedding fairness in decision-making processes, executive departments and agencies (agencies) must recognize and work to redress inequities in their policies and programs that serve as barriers to equal opportunity.

By advancing equity across the Federal Government, we can create opportunities for the improvement of communities that have been historically underserved, which benefits everyone.⁹

As part of this whole of government approach, this Lab Call seeks to encourage the participation of underserved communities and underrepresented^{10,11} groups. Applicants are highly encouraged to include individuals from groups historically underrepresented, in STEM on their project teams. As part of the application, applicants are required to describe how diversity, equity, and inclusion objectives will be incorporated in the project. Specifically, applicants are required to reference, if available, the existing laboratory Diversity, Equity, and Inclusion Plan and describe within the technical volume the actions the

persons of color; members of religious minorities; lesbian, gay, bisexual, transgender, and queer (LGBTQ+) persons; persons with disabilities; persons who live in rural areas; and persons otherwise adversely affected by persistent poverty or inequality. E.O. 13985.

⁹ Executive Order 13985, “Advancing Racial Equity and Support for Underserved Communities Through the Federal Government” (Jan. 20, 2021).

¹⁰ According to the National Science Foundation’s 2019 report titled, “Women, Minorities and Persons with Disabilities in Science and Engineering”, women, persons with disabilities, and underrepresented minority groups—blacks or African Americans, Hispanics or Latinos, and American Indians or Alaska Natives—are vastly underrepresented in the STEM (science, technology, engineering and math) fields that drive the energy sector. That is, their representation in STEM education and STEM employment is smaller than their representation in the U.S. population. <https://ncses.nsf.gov/pubs/nsf19304/digest/about-this-report> For example, in the U.S., Hispanics, African Americans and American Indians or Alaska Natives make up 24 percent of the overall workforce, yet only account for 9 percent of the country’s science and engineering workforce. DOE seeks to inspire underrepresented Americans to pursue careers in energy and support their advancement into leadership positions.

<https://www.energy.gov/articles/introducing-minorities-energy-initiative>

¹¹ Note that Congress recognized in section 305 of the American Innovation and Competitiveness Act of 2017, Public Law 114-329:

(1) [I]t is critical to our Nation’s economic leadership and global competitiveness that the United States educate, train, and retain more scientists, engineers, and computer scientists; (2) there is currently a disconnect between the availability of and growing demand for STEM-skilled workers; (3) historically, underrepresented populations are the largest untapped STEM talent pools in the United States; and (4) given the shifting demographic landscape, the United States should encourage full participation of individuals from underrepresented populations in STEM fields.

Questions about this Lab Call? Email Micro_electronics@ee.doe.gov.

Problems with EERE eXCHANGE? Email EERE-eXCHANGESupport@hq.doe.gov.

Include Lab Call name and number in subject line.

applicant will take to foster a welcoming and inclusive environment, support people from underrepresented groups in STEM, advance equity, and encourage the inclusion of individuals from these groups in the project; and the extent the project activities will be located in or benefit underserved communities.

Because a diverse set of voices at the table in research design and execution has an illustrated impact on innovation, this implementation strategy for the lab-wide plan will be evaluated as part of the technical review process.

Further, to the extent the proposed project will include external partners, the applicant is encouraged to include Minority Serving Institutions¹², Minority Business Enterprises, Minority Owned Businesses, Woman Owned Businesses, Veteran Owned Businesses, or entities located in an underserved community. The Selection Official may consider the inclusion of these types of entities as part of the selection decision.

- **EERE NATIONAL LABORATORY GUIDING PRINCIPLES:** To ensure continued alignment with EERE and AMMTO lab engagement principles, applicants should to the extent possible and appropriate seek lab projects that involve industry engagement.

ii. Topic Area Descriptions

There is only one Topic in this Lab Call.

Topic 1: Lab Seedlings for Devices that contribute at least 10X to EES2.

- Estimated DOE Funding Available: \$4,000,000
- Estimated Number of Projects Expected: Min: 1/ Max: 3
- Estimated Project Duration: Min: 2 years/ Max: 3 years

Topic Background and Opportunity: From January 2021 to January 2022, AMMTO's predecessor –the Advanced Manufacturing Office—led a series of workshops on Semiconductor R&D for Energy Efficiency. This Lab call topic is informed in part by the results of the second workshop in the series that focused on atomic and near-atomic precision manufacturing technologies for more energy-efficient semiconductor

¹² Minority Serving Institutions (MSIs), including Historically Black Colleges and Universities/Other Minority Institutions) as educational entities recognized by the Office of Civil Rights (OCR), U.S. Department of Education, and identified on the OCR's Department of Education U.S. accredited postsecondary minorities' institution list. See <https://www2.ed.gov/about/offices/list/ocr/edlite-minorityinst.html>.

devices¹³. Applicants are strongly encouraged to align proposals with the research directions and approaches articulated in that workshop report. Like that workshop, this topic is focused on R&D to drive ultra-precise control of manufacturing for ultra-energy-efficient (e.g., >10x over today's metal–oxide–semiconductor field-effect transistor (MOSFET)) semiconductor devices. These devices (e.g., transistors used for logic, memory, and communications) are the building blocks for integrated circuits and affect nearly every aspect of our modern lives including some of the fastest growing industries (e.g., telecom, internet, and Internet of Things (IOT)).

AMMTO has been leading an EES2 RD&D Roadmapping¹⁴ effort to enable achievement of the biennial doubling and 1000X increase over EES2 goals. This Lab Call topic is also informed by the Semiconductor Supply Chain Deep Dive Assessment⁶ and the initial public efforts of the Materials and Devices Working Group of the EES2 Roadmap.¹⁵ Device oriented components of other R&D Roadmapping efforts also informed the language of this FOA¹⁶

Technology Focus: In the past DOE- and other government- funded research, the discovery and design of new materials and devices with novel structures, functions, switching physics (e.g., based on unexploited physical phenomena) and other properties often stalled at the proof-of-concept stage. Examples of logic, memory and communications devices are listed in Table 1.

¹³ U.S. DOE, 2021. AMO Semiconductor Workshop 2 - Ultra-Precise Control for Ultra-Efficient Devices, April 21-22, 2021. Report published at https://www.energy.gov/sites/default/files/2022-02/AMO%20Semiconductor%20Workshop%20II%20Report%20FINAL_compliant_02-08-2022.pdf

¹⁴ Two EES2 workshops focused on the goal were a Sept. 14 public workshop with contributed talks on technologies to reach the EES2 goals <https://microelectronics.slac.stanford.edu/amo-microelectronics/presentations> and a Sept 20, EES2 pledge signing and workshop <https://microelectronics.slac.stanford.edu/september-20-2022-pledge>.

¹⁵ For example, among the readings initially assembled by the EES2 Devices working group are: T Alexoudi et al. "Optical RAM and integrated optical memories: a survey," Light Sci Appl 9, 91 (2020). <https://doi.org/10.1038/s41377-020-0325-9>; Gilbert, M.J. "Topological electronics," Commun Phys 4, 70 (2021). <https://doi.org/10.1038/s42005-021-00569-5>; W. Zhicheng et al, "Neuromorphic metasurface," Photon. Res. 8, 46-50 (2020). <https://doi.org/10.1364/PRJ.8.000046>; Onen, Murat et al "Nanosecond protonic programmable resistors for analog deep learning." Science, 377, 6605, 539-543 (2022). <https://doi.org/10.1126/science.abp8064>; Pirie, Harris et al "Topological Phononic Logic." Physical Review Letters, 128, 015501, (2022). <https://doi.org/10.1103/PhysRevLett.128.015501>; A. Talin et al, ECRAM Materials, Devices, Circuits and Architectures: A Perspective. Adv. Mater. 2204771, (2022). <https://doi.org/10.1002/adma.202204771>; Y. Tuchman et al, 2100426, A., A Stacked Hybrid Organic/Inorganic Electrochemical Random-Access Memory for Scalable Implementation. Adv. Electron. Mater., 8, 2100426 (2022). <https://doi.org/10.1002aelm.202100426>; Nikonov, Dmitiri, 2022. "Beyond CMOS Benchmarking", presentation September 14, 2022.

¹⁶ IEEE Heterogeneous Integration Roadmap, 2023 Edition Chapter 16: Emerging Research Devices, released March 2023 at <http://eps.ieee.org/hir>

Device Abbreviation (type)	Full Device Name
TFET (logic)	Tunnel Field Effect Transistor
FeFET (memory and logic)	Ferroelectric Field Effect Transistor
NEMS (memory)	Nano-electro-mechanical system
CNTFET (logic, RF/communications)	Carbon NanoTube Field Effect Transistor
SpinFET (memory)	Spintronic and magnetoelectric FET
2DFET (logic)	2-dimensional material FET includes graphene, dichalcogenides

Table 1: Example Device Types with potential for 10X efficiency compared to MOSFET

In this topic, DOE is only interested in supporting higher TRL R&D on devices that have already been proved as concepts at the lab-scale. In particular, this topic seeks proposals that explore and control novel materials systems and physical properties needed to accelerate commercialization of lab-proven ultra-energy efficient (e.g., 10x vs MOSFET) logic, memory and communications devices including research:

- on synthesis and control of a broad range of electronic and magnetic materials including semiconductors, ferroelectrics and multiferroics leading to accelerated deployment of ultra-energy efficient devices covering computing, communication, and memory/storage;
- on new techniques to synthesize and scale up materials with desired structure, properties, and function. This may include synthesis and scale-up of complex thin films and nanoscale materials with atomic layer-by-layer control;
- to enable scale up of ultra-energy efficient microelectronics devices using industrial scale fabrication that provides a level of precision or control that significantly exceeds that of today's commercial fabs.

Prior research team experience on new device proof-of-concept research is desirable but not required. Because of the urgency of reducing microelectronics energy as soon as possible, for the near- and mid-term the proposed device must be able to be integrated into today's dominant complementary metal-oxide semiconductor technology (CMOS)—i.e. be CMOS¹⁷-compatible.

¹⁷ CMOS is a type of *metal–oxide–semiconductor* FET fabrication process that uses *complementary* pairs of p-type and n-type MOSFETs for logic functions. CMOS-compatible is the standard semiconductor fabrication process.

Not of interest in Topic 1

DOE is not interested in funding applications in this topic that represent evolutionary approaches that provide incremental improvements to currently commercial technologies. R&D focused on devices that have no potential to exceed the energy efficiency of conventional CMOS MOSFET by at least an order of magnitude (e.g., 10x) are not of interest.

Topic 1 Candidate Metrics and Targets:

Targets for devices developed and demonstrated under this topic must be specified in the application. Energy and carbon intensity analyses should be included, including a comparison of the current, commercially available state-of-the-art technology with the proposed advancement. Applications must clearly identify the starting and ending TRL for the project and justify the TRLs assigned. Successful applicants will be required to have a periodic assessment of their metrics during the award to evaluate potential impacts. Applicants must explain how the proposed technology will meet the following metric:

Objective/Goal	Metric	Minimum	Stretch Target	Baseline Performance
Reduce energy consumption	Device Energy per bit	Reduce 10x	Reduce 100X	<i>Applicant Defined (e.g., in attojoules (10^{-18} Joules))</i>

Additional metrics and critical criteria that will lead to successfully meeting the goal above should also be identified. In particular, an estimate of the application efficiency impacts of device innovation must be included—even if it is only a rough estimate based on physical reasoning. In addition, if efficiency improvements decline significantly between the device level and the application level, the applicant must indicate their best estimate of where losses occur and where research may be needed¹⁸. Applicants must identify and justify other appropriate metrics for their technology and clearly indicate how the proposed innovation will satisfy them. Relevant benchmarks/baselines, minimum targets, and stretch targets should be included for each metric; these can also include co-benefits. Examples of applicant-identified metrics include the following:

Objective/Goal	Metric (s)	Minimum	Stretch Target	Baseline Performance
Reduce energy consumption	Energy per instruction (e.g., including interconnect energy use)	Reduce 5X	Reduce 50X	<i>Applicant Defined (e.g., femtojoules (10^{-15} Joules))</i>

¹⁸ An example would be where the energy per bit used in switching is much lower than the energy per application instruction or operation. The physical explanation of the discrepancy might be related to interconnects, or device timing or other causes.

Reduce energy consumption	Energy use per application (e.g., when deployed in compute in memory)	Reduce 3x	Reduce 10x	<i>Applicant Defined (e.g., femtojoules (10^{-15} Joules))</i>
Reduce lifecycle energy impact by lengthening lifetime	Number of cycles (energy of switching during the device lifetime)	Increase 30%	+ 100%	<i>Applicant Defined</i>
Increased device performance (tradeoff)	Switching speed	Same or slightly less than baseline	30%	<i>Applicant Defined</i>
Increase device performance	Endurance (e.g., no. of switches during lifetime)	30% improvement	100%	<i>Applicant Defined</i>
Decrease device manufacturing cost	Kg materials used per layer of processing	10%	30%	<i>Applicant Defined</i>
Decrease device manufacturing cost	Techno-economic analysis of manufacturing process	10%	30%	<i>Applicant Defined</i>
Decrease device manufacturing energy use	Joules used per layer of processing	30%	100%	<i>Applicant Defined</i>
Decrease overall device cost	\$/wafer (product plus lifecycle energy materials use)	30%	100%	<i>Applicant Defined</i>

II. Application Submission and Review Information

A. Application and Submission Details

i. Application Process

To apply to this Lab Call, applicants must register with their lab email address and submit application materials through EERE eXCHANGE at <https://eere-exchange.energy.gov>, EERE's online application portal. Applicants will be required to have a Login.gov account to access EERE eXCHANGE.

As part of the eXCHANGE registration process, users will be directed to create an account in <https://login.gov/>. Please note that the email address associated with

Questions about this Lab Call? Email Micro_electronics@ee.doe.gov.

Problems with EERE eXCHANGE? Email EERE-eXCHANGESupport@hq.doe.gov.

Include Lab Call name and number in subject line.

Login.gov must match the email address associated with the eXCHANGE account. For more information, refer to the Exchange Multi-Factor Authentication (MFA) Quick Guide in the [Manuals section](#) of eXCHANGE.

All submissions must conform to the guidelines for format and length, and be submitted at, or prior to, the deadline listed.

Applicants will be required to include project information and details in eXCHANGE that will be used to develop and accelerate negotiations of FY 2024 Annual Operating Plans (AOPs) if selected. Appendix A provides a worksheet to guide applicants through this process in eXCHANGE. Any information the applicant considers to be of significance for the review process must be included in the proposal, as reviewers will not have access to the AOP development information entered in eXCHANGE.

ii. General Proposal Requirements

Proposals should be formatted for 8.5 x 11 paper, single spaced, and have 1-inch margins on each side. Typeface size should be 12-point font, except tables and figures, which may be in 10-point font.

iii. Proposal Content

Proposal content aligns with content required in the EERE AOP project forms, with additional information to assist reviewers in evaluating technical details. The narrative should build on the information provided as part of the EERE eXCHANGE template.

Applicants must include all content they wish to have reviewed in the proposal (proposal reviewers will not review any information provided in eXCHANGE for AOP development).

Full Applications

- EERE will not review or consider ineligible Full Applications.
- Each Full Application shall be limited to a single concept or technology. Unrelated concepts and technologies shall not be consolidated in a single Full Application.

Full Applications must conform to the following requirements:

SECTION	FILE FORMAT	PAGE LIMIT	FILE NAME
Technical Volume	PDF	25	ControlNumber_LeadOrganization_TechnicalVolume
Resumes	PDF	N/A	ControlNumber_LeadOrganization_Resumes
Letters of Commitment (if applicable)	PDF	N/A	ControlNumber_LeadOrganization_LOCs

Questions about this Lab Call? Email Micro_electronics@ee.doe.gov.

Problems with EERE eXCHANGE? Email EERE-eXCHANGESupport@hq.doe.gov.

Include Lab Call name and number in subject line.

Summary/Abstract for Public Release	PDF	1	ControlNumber_LeadOrganization_Summary
Summary Slide	MS PowerPoint	1	ControlNumber_LeadOrganization_Slide
DOE Work Proposal for FFRDC (if applicable) (see DOE O 412.1A, Attachment 3)	PDF	15	ControlNumber_LeadOrganization_WP
Authorization from cognizant Contracting Officer for FFRDC (if applicable)	PDF	N/A	ControlNumber_LeadOrganization_FFRDCAuth
SF-LLL Disclosure of Lobbying Activities	PDF	N/A	ControlNumber_LeadOrganization_SF-LLL
Foreign Entities and Foreign Work Waiver (if applicable)	PDF	N/A	ControlNumber_LeadOrganization_Waiver
Data Management Plan	MS Word	5	ControlNumber_LeadOrganization_DMP
Diversity, Equity, Inclusion, and Accessibility (DEIA) Implementation Plan	PDF	5	ControlNumber_LeadOrganization_DEIAP

Technical Volume

The Technical Volume must be submitted in PDF format. The Technical Volume must conform to the following content and form requirements, including maximum page lengths. If applicants exceed the maximum page lengths indicated below, EERE will review only the authorized number of pages and disregard any additional pages. Save the Technical Volume in a single PDF file using the following convention for the title "ControlNumber_LeadOrganization_TechnicalVolume".

Applicants must provide sufficient citations and references to the primary research literature to justify the claims and approaches made in the Technical Volume. However, EERE and reviewers are under no obligation to review cited sources.

The Technical Volume to the Full Application may not be more than 25 pages, including the cover page, table of contents, and all citations, charts, graphs, maps, photos, or other graphics, and must include all of the information in the table below. The applicant

Questions about this Lab Call? Email Micro_electronics@ee.doe.gov.

Problems with EERE eXCHANGE? Email EERE-eXCHANGESupport@hq.doe.gov.

Include Lab Call name and number in subject line.

should consider the weighting of each of the evaluation criteria when preparing the Technical Volume.

The Technical Volume must conform to the following content requirements:

SECTION / PAGE LIMIT	DESCRIPTION
Cover Page	The cover page should include the project title, the specific Lab Call Topic Area being addressed, both the technical and business points of contact, names of all team member organizations, and any statements regarding confidentiality.
Project Overview (Approximately 10% of the Technical Volume)	The Project Overview should contain the following information: <ul style="list-style-type: none"> Background: The applicant should discuss the background of their organization, including the history, successes, and current research and development status (i.e., the technical baseline) relevant to the technical topic being addressed in the Full Application. Project Goal: The applicant should explicitly identify the targeted improvements to the baseline technology and the critical success factors in achieving that goal. DOE Impact: The applicant should discuss the impact that DOE funding would have on the proposed project. Applicants should specifically explain how DOE funding, relative to prior, current, or anticipated funding from other public and private sources, is necessary to achieve the project objectives.
Technical Description, Innovation, and Impact (Approximately 30% of the Technical Volume)	The Technical Description should contain the following information: <ul style="list-style-type: none"> Relevance and Outcomes: The applicant should provide a detailed description of the technology, including the scientific and other principles and objectives that will be pursued during the project. This section should describe the relevance of the proposed project to the goals and objectives of the Lab Call, including the potential to meet specific DOE technical targets or other relevant performance targets. The applicant should clearly specify the expected outcomes of the project. Feasibility: The applicant should demonstrate the technical feasibility of the proposed technology and capability of achieving the anticipated performance targets, including a description of previous work done and prior results. Innovation and Impacts: The applicant should describe the current state-of-the-art in the applicable field, the specific innovation of the proposed technology, the advantages of proposed technology over current and emerging technologies, and the overall impact on advancing the state-of-the-art/technical baseline if the project is successful.
Workplan and Market Transformation Plan (Approximately 40% of the Technical Volume)	The Workplan should include a summary of the Project Objectives, Technical Scope, Work Breakdown Structure (WBS), Milestones, Go/No-Go Decision Points, and Project Schedule. A detailed SOPO is separately requested. The Workplan should contain the following information:

Questions about this Lab Call? Email Micro_electronics@ee.doe.gov.

Problems with EERE eXCHANGE? Email EERE-eXCHANGESupport@hq.doe.gov.

Include Lab Call name and number in subject line.

	<ul style="list-style-type: none"> • Project Objectives: The applicant should provide a clear and concise (high-level) statement of the goals and objectives of the project as well as the expected outcomes. • Technical Scope Summary: The applicant should provide a summary description of the overall work scope and approach to achieve the objective(s). The overall work scope is to be divided by performance periods that are separated by discrete, approximately annual decision points (see below for more information on Go/No-Go decision points). The applicant should describe the specific expected end result of each performance period. • WBS and Task Description Summary: The Workplan should describe the work to be accomplished and how the applicant will achieve the milestones, will accomplish the final project goal(s), and will produce all deliverables. The Workplan is to be structured with a hierarchy of performance period (approximately annual), task and subtasks, which is typical of a standard WBS for any project. The Workplan shall contain a concise description of the specific activities to be conducted over the life of the project. The description shall be a full explanation and disclosure of the project being proposed (i.e., a statement such as “we will then complete a proprietary process” is unacceptable). It is the applicant’s responsibility to prepare an adequately detailed task plan to describe the proposed project and the plan for addressing the objectives of this Lab Call. The summary provided should be consistent with the SOPO. The SOPO will contain a more detailed description of the WBS and tasks. • Milestone Summary: The applicant should provide a summary of appropriate milestones throughout the project to demonstrate success. A milestone may be either a progress measure (which can be activity based) or a SMART technical milestone. SMART milestones should be Specific, Measurable, Achievable, Relevant, and Timely, and must demonstrate a technical achievement rather than simply completing a task. Unless otherwise specified in the Lab Call, the minimum requirement is that each project must have at least one milestone per quarter for the duration of the project with at least one SMART technical milestone per year (depending on the project, more milestones may be necessary to comprehensively demonstrate progress). The applicant should also provide the means by which the milestone will be verified. The summary provided should be consistent with the Milestone Summary Table in the SOPO. • Go/No-Go Decision Points: The applicant should provide a summary of project-wide Go/No-Go decision points at appropriate points in the Workplan. A Go/No-Go decision point is a risk management tool and a project management best practice to ensure that, for the current phase or period of performance, technical success is definitively achieved and potential for success in future phases or periods of performance is evaluated, prior to actually beginning the execution of future phases. At a minimum,
--	--

Questions about this Lab Call? Email Micro_electronics@ee.doe.gov.

Problems with EERE eXCHANGE? Email EERE-eXCHANGESupport@hq.doe.gov.

Include Lab Call name and number in subject line.

	<p>each project must have at least one project-wide Go/No-Go decision point for each budget period (12 to 18-month period) of the project. The applicant should also provide the specific technical criteria to be used to evaluate the project at the Go/No-Go decision point. The summary provided should be consistent with the SOPO. Go/No-Go decision points are considered “SMART” and can fulfill the requirement for an annual SMART milestone.</p> <ul style="list-style-type: none"> ● End of Project Goal: The applicant should provide a summary of the end of project goal(s). At a minimum, each project must have one SMART end of project goal. The summary provided should be consistent with the SOPO. ● Project Schedule (Gantt Chart or similar): The applicant should provide a schedule for the entire project, including task and subtask durations, milestones, and Go/No-Go decision points. ● Project Management: The applicant should discuss the team’s proposed management plan, including the following: <ul style="list-style-type: none"> ○ The overall approach to and organization for managing the work ○ The roles of each project team member ○ Any critical handoffs/interdependencies among project team members ○ The technical and management aspects of the management plan, including systems and practices, such as financial and project management practices ○ The approach to project risk management ○ A description of how project changes will be handled ○ If applicable, the approach to Quality Assurance/Control ○ How communications will be maintained among project team members ● Market Transformation Plan: The applicant should provide a market transformation plan, including the following: <ul style="list-style-type: none"> ○ Identification of target market, competitors, and distribution channels for proposed technology along with known or perceived barriers to market penetration, including a mitigation plan ○ Identification of a product development and/or service plan, commercialization timeline, financing, product marketing, legal/regulatory considerations including intellectual property, infrastructure requirements, data dissemination, and product distribution.
Technical Qualifications and Resources (Approximately 20% of the Technical Volume)	<p>The Technical Qualifications and Resources should contain the following information:</p> <ul style="list-style-type: none"> ● Describe the project team’s unique qualifications and expertise, including those of key subrecipients. ● Describe the project team’s existing equipment and facilities that will facilitate the successful completion of the proposed project; include a justification of any new equipment or facilities requested as part of the project.

Questions about this Lab Call? Email Micro_electronics@ee.doe.gov.

Problems with EERE eXCHANGE? Email EERE-eXCHANGESupport@hq.doe.gov.

Include Lab Call name and number in subject line.

	<ul style="list-style-type: none"> • This section should also include relevant, previous work efforts, demonstrated innovations, and how these enable the applicant to achieve the project objectives. • Describe the time commitment of the key team members to support the project. • Describe the technical services to be provided by DOE/NNSA FFRDCs, if applicable. • For multi-organizational or multi-investigator projects, describe succinctly: <ul style="list-style-type: none"> ○ The roles and the work to be performed by each PI and Key Participant; ○ Business agreements between the applicant and each PI and Key Participant; ○ How the various efforts will be integrated and managed; ○ Process for making decisions on scientific/technical direction; ○ Publication arrangements; ○ Intellectual Property issues; and ○ Communication plans
--	--

Resumes

Applicants are required to submit 3-page resumes for key participating team members. Save the resumes in a single PDF file using the following convention for the title "ControlNumber_LeadOrganization_Resumes".

Letters of Commitment (if applicable)

If applicable, submit letters of commitment from all subrecipient and third-party cost share providers. If applicable, also include any letters of commitment from partners/end users (1-page maximum per letter). Save the letters of commitment in a single PDF file using the following convention for the title "ControlNumber_LeadOrganization_LOCs".

Summary/Abstract for Public Release

Applicants are required to submit a single page summary/abstract of their project. The project summary/abstract must contain a summary of the proposed activity suitable for dissemination to the public. It should be a self-contained document that identifies the name of the applicant, the project director/principal investigator(s), the project title, the objectives of the project, a description of the project, including methods to be employed, the potential impact of the project (e.g., benefits, outcomes), and major participants (for collaborative projects). This document must not include any proprietary or sensitive business information as DOE may make it available to the public after selections are made. The project summary must not exceed a single page when printed using standard 8.5 x 11 paper with 1" margins (top, bottom, left, and

Questions about this Lab Call? Email Micro_electronics@ee.doe.gov.

Problems with EERE eXCHANGE? Email EERE-eXCHANGESupport@hq.doe.gov.

Include Lab Call name and number in subject line.

right) with font not smaller than 12 point. Save the Summary for Public Release in a single PDF file using the following convention for the title “ControlNumber_LeadOrganization_Summary”.

Summary Slide

Applicants are required to provide a single MS Powerpoint slide summarizing the proposed project. This slide is used during the evaluation process.

The Summary Slide template requires the following information:

- A technology summary;
- A description of the technology’s impact;
- Proposed project goals;
- Any key graphics (illustrations, charts and/or tables);
- The project’s key idea/takeaway;
- Project title, prime recipient, Principal Investigator, and Key Participant information; and
- Requested EERE funds and proposed applicant cost share.

Save the Summary Slide in a single page MS Powerpoint file using the following convention for the title “ControlNumber_LeadOrganization_Slide”.

Budget for DOE/NNSA FFRDC (if applicable)

If a DOE/NNSA FFRDC contractor is to perform a portion of the work, the applicant must provide a DOE WP in accordance with the requirements in DOE Order 412.1A, Work Authorization System, Attachment 3, available at

<https://www.directives.doe.gov/directives-documents/400-series/0412.1-BOrder-a-chg1-AdmChg> Save the WP in a single PDF file using the following convention for the title “ControlNumber_LeadOrganization_WP”.

Authorization for non-DOE/NNSA or DOE/NNSA FFRDCs (if applicable)

The federal agency sponsoring the FFRDC must authorize in writing the use of the FFRDC on the proposed project and this authorization must be submitted with the application. The use of a FFRDC must be consistent with the contractor’s authority under its award. Save the Authorization in a single PDF file using the following convention for the title “ControlNumber_LeadOrganization_FFRDCAuth”.

SF-LLL: Disclosure of Lobbying Activities

Prime recipients and subrecipients may not use any federal funds to influence or attempt to influence, directly or indirectly, congressional action on any legislative or appropriation matters.

Prime recipients and subrecipients are required to complete and submit SF-LLL, “Disclosure of Lobbying Activities” (<https://www.grants.gov/web/grants/forms/sf-424->

Questions about this Lab Call? Email Micro_electronics@ee.doe.gov.

Problems with EERE eXCHANGE? Email EERE-eXCHANGESupport@hq.doe.gov.

Include Lab Call name and number in subject line.

[individual-family.html](#)) to ensure that non-federal funds have not been paid and will not be paid to any person for influencing or attempting to influence any of the following in connection with the application:

- An officer or employee of any federal agency;
- A Member of Congress;
- An officer or employee of Congress; or
- An employee of a Member of Congress.

Save the SF-LLL in a single PDF file using the following convention for the title
“ControlNumber_LeadOrganization_SF-LLL”

[Waiver Requests: Foreign Entities and Foreign Work \(if applicable\)](#)

1. Foreign Entity Participation:

All lab partners receiving funding under this Lab Call must be incorporated (or otherwise formed) under the laws of a State or territory of the United States. To request a waiver of this requirement, the applicant must submit an explicit waiver request in the Full Application. Appendix B lists the necessary information that must be included in a request to waive this requirement.

2. Performance of Work in the United States (Foreign Work Waiver)

All work funded by EERE must be performed in the United States. This requirement does not apply to the purchase of supplies and equipment, so a waiver is not required for foreign purchases of these items. However, the prime recipient should make every effort to purchase supplies and equipment within the United States. Appendix B lists the necessary information that must be included in a foreign work waiver request.

Save the Waivers in a single PDF file using the following convention for the title
“ControlNumber_LeadOrganization_Waiver”.

[Data Management Plan](#)

Each proposal under this Lab Call must have a data management plan (DMP). A DMP explains how, when appropriate, data generated in the course of the proposed work will be shared and preserved in order to validate the results of the work or how the results could be validated if the data is not shared or preserved. The DMP must provide a plan for making all research data displayed in publications resulting from the proposed work digitally accessible at the time of publications.

A lab may have a previously DOE approved DMP, such as a lab-wide DMP, and to the extent that the DMP applies to the proposal submitted under this Lab Call, the lab may rely on that DMP to satisfy the DMP requirement of this Lab Call. If there is no existing DMP that can apply and the applicant fails to submit a DMP as part of the proposal, then the default DMP for the proposal is the following:

Questions about this Lab Call? Email Micro_electronics@ee.doe.gov.

Problems with EERE eXCHANGE? Email EERE-eXCHANGESupport@hq.doe.gov.

Include Lab Call name and number in subject line.

For any publication that includes results of the project, the underlying research data will be made available according to the policies of the publishing media. Where no such policy exists, the applicant must indicate on the publication a means for requesting and digitally obtaining the underlying research data. This includes the research data necessary to validate any results, conclusions, charts, figures, images in the publications.

Save the DMP in a single Microsoft Word file using the following convention for the title “ControlNumber_LeadOrganization_DMP”.

Diversity, Equity, Inclusion, and Accessibility (DEIA) Implementation Plan

As part of the application, applicants are required to describe how DEIA objectives will be incorporated in the project. Specifically, applicants are required to submit a description of how the project will support or implement the lab-wide DEIA Plan and describe the actions the applicant will take to foster a welcoming and inclusive environment, support people from groups underrepresented in STEM, advance equity, and encourage the inclusion of individuals from these groups in the project; and the extent the project activities will be located in or benefit underserved communities. The plan should include SMART milestones supported by metrics to measure the success of the proposed actions.

The DEIA Implementation plan should reference the lab DEIA plan if available, and contain the following information:

- Equity Impacts: the impacts of the proposed project on underserved communities, including social and environmental impacts.
- Benefits: The overall benefits of the proposed project, if funded, to underserved communities; and
- How diversity, equity, and inclusion objectives will be incorporated in the project.

The following is a non-exhaustive list of actions that can serve as examples of ways the proposed project could incorporate diversity, equity, and inclusion elements. These examples should not be considered either comprehensive or prescriptive. Applicants are encouraged to propose appropriate actions not covered by these examples.

- a. Diversity on the research team
 - i. Include persons from groups underrepresented in STEM as PI, co-PI, and/or other senior personnel;
 - ii. Include persons from groups underrepresented in STEM as student researchers or post-doctoral researchers;

- iii. Implement evidence-based, diversity-focused education programs (such as implicit bias training for staff) in your organization;
- iv. Identify Minority Business Enterprises, Minority Owned Businesses, Woman Owned Businesses and Veteran Owned Businesses to solicit as vendors and sub-contractors for bids on supplies, services and equipment
- v. Include faculty or students from Minority Serving Institutions as PI/co-PI, senior personnel, and/or student researchers;
- vi. Enhance or collaborate with existing diversity programs at your home organization and/or nearby organizations;
- vii. Collaborate with students, researchers, and staff in Minority Serving Institutions;
- b. Explicit diversity in research impact
 - i. Illustrated outcome impact in underserved communities
 - ii. Disseminate results of research and development in Minority Serving Institutions or other appropriate institutions serving underserved communities;
- c. explicit diversity in research design. Inclusion of a broad community, academic, policymaking staff in research design and execution phase

Save the DEIA Implementation Plan in a single PDF file using the following convention for the title "ControlNumber_LeadOrganization_DEIAP"

Treatment of Application Information

Proprietary Information

In general, DOE will use data and other information contained in proposals only for evaluation purposes, unless such information is generally available to the public or is already the property of the government.

Proposals should not include trade secrets or commercial or financial information that is privileged or confidential unless such information is necessary to convey an understanding of the proposed project or to comply with a requirement in the Lab Call.

Proposals containing confidential, proprietary, or privileged information must be conspicuously marked as described below. Failure to comply with these marking requirements may result in the disclosure of the unmarked information under the Freedom of Information Act or otherwise. The U.S. Federal Government is not liable for the disclosure or use of unmarked information, and may use or disclose such information for any purpose.

If a proposal contains confidential, proprietary, or privileged information, it must include a cover sheet marked as follows identifying the specific pages containing confidential, proprietary, or privileged information:

Questions about this Lab Call? Email Micro_electronics@ee.doe.gov.

Problems with EERE eXCHANGE? Email EERE-eXCHANGESupport@hq.doe.gov.

Include Lab Call name and number in subject line.

1. Notice of Restriction on Disclosure and Use of Data:

Pages [List Applicable Pages] of this proposal may contain confidential, proprietary, or privileged information that is exempt from public disclosure. Such information shall be used or disclosed only for the purposes described in this Lab Call. The government may use or disclose any information that is not appropriately marked or otherwise restricted, regardless of source. In addition, (1) the header and footer of every page that contains confidential, proprietary, or privileged information must be marked as follows: “Contains Confidential, Proprietary, or Privileged Information Exempt from Public Disclosure” and (2) every line and paragraph containing proprietary, privileged, or trade secret information must be clearly marked with double brackets or highlighting.

B. Application Review Details

i. Merit Review and Selection Process

Upon receipt and review for initial compliance with requirements, all proposals received in eXCHANGE by the deadline will undergo a thorough technical review. AMMTO will use expert reviewers familiar with the AMMTO portfolio, goals, and objectives. AMMTO will collect and collate review scores and comments for use in making final project selections. The AMMTO Selection Official will consider the merit review results to make the final project selections. For transparency, AMMTO will provide summaries of the review results to assist labs in understanding how their submission reviewed and aid in improving future work.

ii. Technical Review Criteria

Final Applications

Applications will be evaluated against the merit review criteria shown below:

Criterion 1: Technical Merit, Innovation, and Impact (50%)

This criterion involves consideration of the following factors:

Technical Merit and Innovation

- Extent to which the proposed technology or process is innovative;
- Degree to which the current state of the technology and the proposed advancement are clearly described;
- Extent to which the application specifically and convincingly demonstrates how the applicant will move the state-of-the-art to the proposed advancement; and
- Sufficiency of technical detail in the application to assess whether the proposed work is scientifically meritorious and revolutionary, including relevant data, calculations and discussion of prior work in the literature with analyses that support the viability of the proposed work.

Impact of Technology Advancement

- How the project supports the topic area objectives and target specifications and metrics; and
- The potential impact of the project on advancing the state-of-the-art.

Criterion 2: Project Research and Market Transformation Plan (25%)

This criterion involves consideration of the following factors:

Research Approach, Workplan and SOPO

- Degree to which the approach and critical path have been clearly described and thoughtfully considered; and
- Degree to which the task descriptions are clear, detailed, timely, and reasonable, resulting in a high likelihood that the proposed Workplan and SOPO will succeed in meeting the project goals.

Identification of Technical Risks

- Discussion and demonstrated understanding of the key technical risk areas involved in the proposed work and the quality of the mitigation strategies to address them.

Baseline, Metrics, and Deliverables

- The level of clarity in the definition of the baseline, metrics, and milestones; and
- Relative to a clearly defined experimental baseline, the strength of the quantifiable metrics, milestones, and a mid-point deliverable defined in the application, such that meaningful interim progress will be made.

Market Transformation Plan

- Identification of target market, competitors, and distribution channels for proposed technology along with known or perceived barriers to market penetration, including mitigation plan; and
- Comprehensiveness of market transformation plan including but not limited to product development and/or service plan, commercialization timeline, financing, product marketing, legal/regulatory considerations including intellectual property, infrastructure requirements, and product distribution.

Criterion 3: Team and Resources (15%)

This criterion involves consideration of the following factors:

- The capability of the Principal Investigator(s) and the proposed team to address all aspects of the proposed work with a high probability of success. The qualifications, relevant expertise, and time commitment of the individuals on the team;
- The sufficiency of the facilities to support the work;

Questions about this Lab Call? Email Micro_electronics@ee.doe.gov.

Problems with EERE eXCHANGE? Email EERE-eXCHANGESupport@hq.doe.gov.

Include Lab Call name and number in subject line.

- The degree to which the proposed consortia/team demonstrates the ability to facilitate and expedite further development and commercial deployment of the proposed technologies;
- The level of participation by project participants as evidenced by letter(s) of commitment and how well they are integrated into the Workplan; and
- The reasonableness of the budget and spend plan for the proposed project and objectives.

Criterion 4: Diversity, Equity, Inclusion, Accessibility (10%)

This criterion involves consideration of the following factors:

- The quality and manner in which the measures incorporate diversity, equity and inclusion goals in the project; and
- Extent to which the project benefits underserved communities.
- Extent to which concrete steps to be taken to ensure DEI are included

iii. Selection for Award Negotiation

AMMTO carefully considers all of the information obtained through the proposal process and makes an independent assessment of each compliant and responsive proposal based on the criteria set forth in this Lab Call. AMMTO may select or not select a proposal for negotiations. AMMTO may also postpone a final selection determination on one or more proposals until a later date, subject to availability of funds and other factors. AMMTO will notify applicants if they are, or are not, selected for award negotiation.

iv. Selection Notification

AMMTO anticipates completing the project selection process and notifying labs of selections during the month of August 2023 (**subject to change**).

AMMTO will notify lab leads of selection results from Micro.electronics@ee.doe.gov and will provide lab leads with summaries of anonymized review comments for each proposal submitted.

v. Questions and Agency Contacts

Specific questions about this Lab Call should be submitted via e-mail to Micro.electronics@ee.doe.gov. To ensure fairness across all labs, individual AMMTO staff cannot answer questions while the Lab Call remains open. To keep all labs informed, AMMTO will post all questions and answers on EERE eXCHANGE.

Questions about this Lab Call? Email Micro.electronics@ee.doe.gov.

Problems with EERE eXCHANGE? Email EERE-eXCHANGESupport@hq.doe.gov.

Include Lab Call name and number in subject line.

Appendix A: Lab Call Full Application Worksheet for eXCHANGE

Lab Call Full Application Worksheet

IMPORTANT: This document is provided as a courtesy to allow Lab Call applicants to collaborate offline to develop Full Applications for Lab Calls. All information must be entered into the eXCHANGE system and cannot be submitted with this document.

Please contact ITSIHelp@ee.doe.gov with any questions.

Project General Information

Control Number:

Applicant (Name and Email):

Organization Name:

Project Title:

Topic:

Project Start Date:

Project End Date:

Partner Laboratories:

Partner Laboratory	Email	First Name	Last Name

Is this a continuation of an existing project?

WBS Number:

Fiscal Year Existing Project:

Project Overview (Multi-year):

Project Objectives (Multi-year):

Contact Information

Lab Lead Point of Contact and Business Contact Information

Name:

Email:

Title:

Address:

Questions about this Lab Call? Email Micro_electronics@ee.doe.gov.

Problems with EERE eXCHANGE? Email EERE-eXCHANGESupport@hq.doe.gov.

Include Lab Call name and number in subject line.

Phone:

Fax:

Financials

Please add a separate table for each partner laboratory.

Lead Laboratory Name:

Year	Planned Project Costs
2021	
2022	
2023	
Subtotal	

Partner Laboratory (If Applicable) Name:

Year	Planned Project Costs
2021	
2022	
2023	
Subtotal	

Total Planned Project Costs:

Questions about this Lab Call? Email Micro_electronics@ee.doe.gov.

Problems with EERE eXCHANGE? Email EERE-eXCHANGESupport@hq.doe.gov.

Include Lab Call name and number in subject line.

Performers

Please add a separate table for each partner laboratory.

Lead Laboratory Name:

Subcontractor Name	Sub Type	Start Date	End Date	2021 Planned Costs	2022 Planned Costs	2023 Planned Costs	Total Funding
Subcontractor Subtotal							

Partner Laboratory (If Applicable) Name:

Subcontractor Name	Sub Type	Start Date	End Date	2021 Planned Costs	2022 Planned Costs	2023 Planned Costs	Total Funding
Subcontractor Subtotal							

Total Planned Project Costs:

Questions about this Lab Call? Email Micro_electronics@ee.doe.gov.

Problems with EERE eXCHANGE? Email EERE-eXCHANGESupport@hq.doe.gov.

Include Lab Call name and number in subject line.

Project Plan

Project Tasks:

Task Number	Title	Description	Team Members	Planned Costs	Start Date	End Date

Project Milestones:

Item Number	Type	Title	Description	End Date	Team Members	Criteria

Questions about this Lab Call? Email Micro.electronics@ee.doe.gov.

Problems with EERE eXCHANGE? Email EERE-eXCHANGESupport@hq.doe.gov.

Include Lab Call name and number in subject line.

Risks

Project Tasks:

Risk Name	Description	Response Plan	Severity	Probability	Response	Source	Classification	Team Members	Target Completion Date

Questions about this Lab Call? Email Micro_electronics@ee.doe.gov.

Problems with EERE eXCHANGE? Email EERE-eXCHANGESupport@hq.doe.gov.

Include Lab Call name and number in subject line.

Modalities/TRL (see Appendix C for EERE definitions of TRLs)

Modalities:

Modality Number	Modality	FY21 Weight (%)	FY21 Planned Costs (\$)
Total:			

Current TRL of the proposed technology (1-9):

Estimated TRL the technology will reach at project end (2-9):

Questions about this Lab Call? Email Micro_electronics@ee.doe.gov.

Problems with EERE eXCHANGE? Email EERE-eXCHANGESupport@hq.doe.gov.

Include Lab Call name and number in subject line.

Project Impacts

Deliverable/Product or "Output" Description:

Audience/Customer:

Audience/Customer Use:

Communications/Outreach Strategy:

Does this project involve significant industry engagement?

Description of Engagement:

Associated CRADAs?

CRADA Text

Questions about this Lab Call? Email Micro_electronics@ee.doe.gov.

Problems with EERE eXCHANGE? Email EERE-eXCHANGESupport@hq.doe.gov.

Include Lab Call name and number in subject line.

Appendix B: Waiver Requests and Approval Processes:

- 1. Foreign Entity Participation as Lab Partners; and**
- 2. Performance of Work in the United States (Foreign Work Waiver)**

1. Waiver for Foreign Entity Participation as the Prime Recipient

Many of the technology areas DOE funds fall in the category of critical and emerging technologies (CETs). CETs are a subset of advanced technologies that are potentially significant to United States national and economic security.³¹ Lab partners (industry and/or organization partners that are **not** DOE/National Nuclear Security Agency (NNSA), Federally Funded Research and Development Centers (FFRDCs) must be organized and chartered or incorporated (or otherwise formed) under the laws of a state or territory of the United States; have majority domestic ownership and control; and have a physical location for business operations in the United States.

To request a waiver of this requirement, an applicant must submit an explicit waiver request in the Full Application. Foreign entities seeking to participate in a project funded under this Lab Call must demonstrate to the satisfaction of DOE that:

Waiver Criteria

Foreign entities seeking to participate in a project funded under this Lab Call must demonstrate to the satisfaction of DOE that:

- a. Its participation is in the best interest of U.S. industry and U.S. economic development;
- b. The project team has appropriate measures in place to control sensitive information and protect against unauthorized transfer of scientific and technical information;
- c. Adequate protocols exist between the U.S. subsidiary and its foreign parent organization to comply with export control laws and any obligations to protect proprietary information from the foreign parent organization;
- d. The work is conducted within the U.S. and the entity acknowledges and demonstrates that it has the intent and ability to comply with the U.S. competitiveness provision; and
- e. The foreign entity will satisfy other conditions that DOE may necessary to protect U.S. government interests.

Content for Waiver Request

A foreign entity waiver request must include the following:

Questions about this Lab Call? Email Micro_electronics@ee.doe.gov.

Problems with EERE eXCHANGE? Email EERE-eXCHANGESupport@hq.doe.gov.

Include Lab Call name and number in subject line.

- a. Information about the entity: name, point of contact, and proposed type of involvement in the project;
- b. Country of incorporation, the extent of the ownership/level control by foreign entities, whether the entity is state owned or controlled, a summary of the ownership breakdown of the foreign entity, and the percentage of ownership/control by foreign entities, foreign shareholders, foreign state, or foreign individuals;
- c. The rationale for proposing a foreign entity participate (must address criteria above);
- d. A description of the project's anticipated contributions to the U.S. economy;
 - How the project will benefit the U.S., including manufacturing, contributions to employment in the U.S. and growth in new markets and jobs in the U.S.;
 - How the project will promote manufacturing of products and/or services in the U.S.;
- e. A description of how the foreign entity's participation is essential to the project;
- f. A description of the likelihood of Intellectual Property (IP) being created from the work and the treatment of any such IP; and
- g. Countries where the work will be performed. (Note: If any work is proposed to be conducted outside the U.S., the applicant must also complete a separate request foreign work waiver).

DOE may also require:

- A risk assessment with respect to IP and data protection protocols that includes the export control risk based on the data protection protocols, the technology being developed, and the foreign entity and country. These submissions could be prepared by the project lead (if not the prime recipient), but the prime recipient must make a representation to DOE as to whether it believes the data protection protocols are adequate and make a representation of the risk assessment – high, medium, or low risk of data leakage to a foreign entity.
- Additional language be added to any agreement or subagreement to protect IP, mitigate risk, or other related purposes.

DOE may require additional information before considering the waiver request.

DOE's decision concerning a waiver request is not appealable.

2. Waiver for Performance of Work in the United States (Foreign Work Waiver)

All work funded under this Lab Call must be performed in the United States. To seek a waiver of the Performance of Work in the United States requirement, the lab partner must submit an explicit waiver request in the Full Application. A separate waiver request must be submitted for each entity proposing performance of work outside of the United States.

Overall, a waiver request must demonstrate to the satisfaction of DOE that it would further the purposes of this Lab Call and is otherwise in the economic interests of the United States to perform work outside of the United States. A request for a foreign work waiver must include the following:

1. The rationale for performing the work outside the U.S. (“foreign work”);
2. A description of the work proposed to be performed outside the U.S.;
3. An explanation as to how the foreign work is essential to the project;
4. A description of the anticipated benefits to be realized by the proposed foreign work and the anticipated contributions to the U.S. economy;
5. The associated benefits to be realized and the contribution to the project from the foreign work;
6. How the foreign work will benefit U.S. research, development and manufacturing, including contributions to employment in the U.S. and growth in new markets and jobs in the U.S.;
7. How the foreign work will promote domestic American manufacturing of products and/or services;
8. A description of the likelihood of Intellectual Property (IP) being created from the foreign work and the treatment of any such IP;
9. The total estimated cost (DOE and recipient cost share) of the proposed foreign work;
10. The countries in which the foreign work is proposed to be performed; and
11. The name of the entity that would perform the foreign work. Information about the entity(ies) involved in the work proposed to be conducted outside the U.S. (i.e., the entity seeking a waiver and the entity(ies) that will conduct the work).

DOE may require additional information before considering the waiver request.

DOE’s decision concerning a waiver request is not appealable.

Appendix C: EERE Definition of Technology Readiness Levels

TRL 1:	Basic principles observed and reported
TRL 2:	Technology concept and/or application formulated
TRL 3:	Analytical and experimental critical function and/or characteristic proof of concept
TRL 4:	Component and/or breadboard validation in a laboratory environment
TRL 5:	Component and/or breadboard validation in a relevant environment
TRL 6:	System/subsystem model or prototype demonstration in a relevant environment
TRL 7:	System prototype demonstration in an operational environment
TRL 8:	Actual system completed and qualified through test and demonstrated
TRL 9:	Actual system proven through successful mission operations

Questions about this Lab Call? Email Micro_electronics@ee.doe.gov.
Problems with EERE eXCHANGE? Email EERE-eXCHANGESupport@hq.doe.gov.
Include Lab Call name and number in subject line.